Design Techniques for VHF & UHF LNAs

by

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The VHF and L-Band LNA Design Challenge

- **Today's transistors have very low noise figures and very high gain**
- **High gain contributes to stability problems and decreased input intercept point**
- **Minimum input VSWR and minimum noise figure will generally not occur simultaneously with same matching network. Use of source inductance may help but too much may cause instability**
- **Generally S parameters taken down to 500 MHz and noise parameters taken down to 2 GHz - Extrapolation required for VHF LNA design**

ATF-3X143 Series of PHEMTs

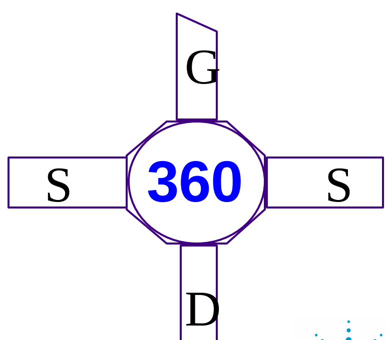
PHEMT technology for higher performance especially at cellular and PCS frequencies

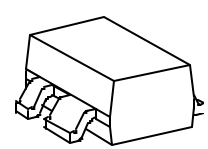
Small plastic surface mount packaging

Various gate widths 400u / 800u / 1600 u

At lower frequencies, I.e. 2 GHz or less, larger gate widths offer lower gain and lower impedances which can contribute to improved stability and lower matching circuit losses

ATF-36077 – 200 u





ATF-35143 – 400 u ATF-34143 – 800 u ATF-33143 – 1600 u

What about S-parameters?!??!

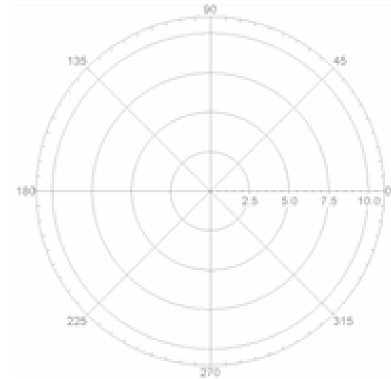
A three-terminal two-port, such as the FET shown, has four S-parameters.

S_{nn} = voltage reflection coefficient, both amplitude and phase relative to 50 W source impedance

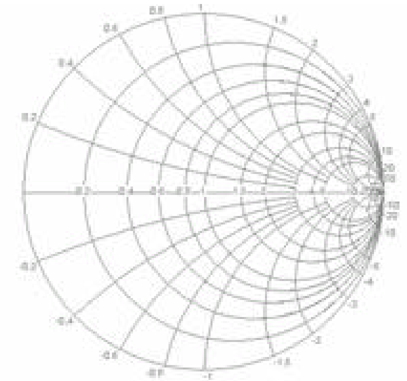
S_{21} and S_{12} are commonly displayed on a polar chart.

S_{11} = G_{input} displayed on Smith chart

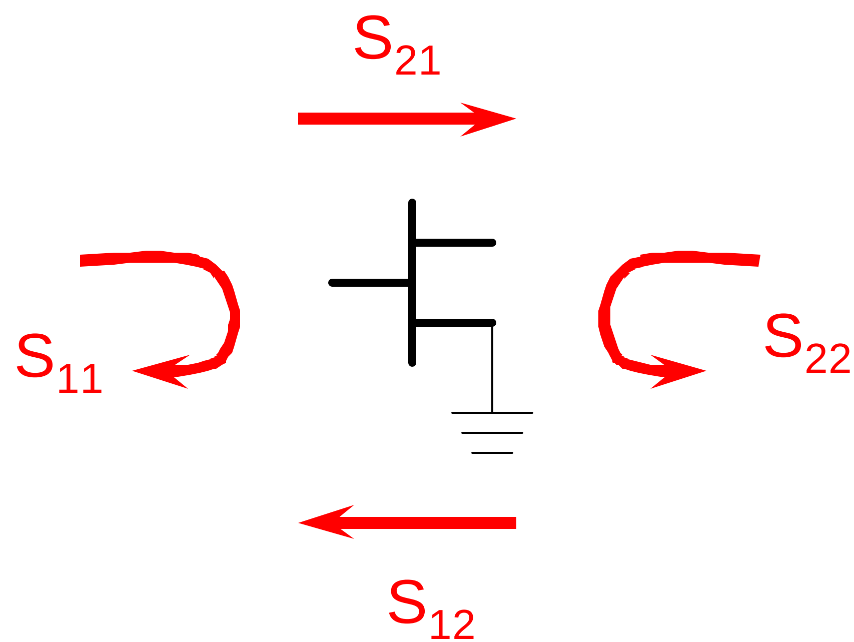
S_{22} = G_{output} displayed on Smith chart



Polar chart



Smith chart



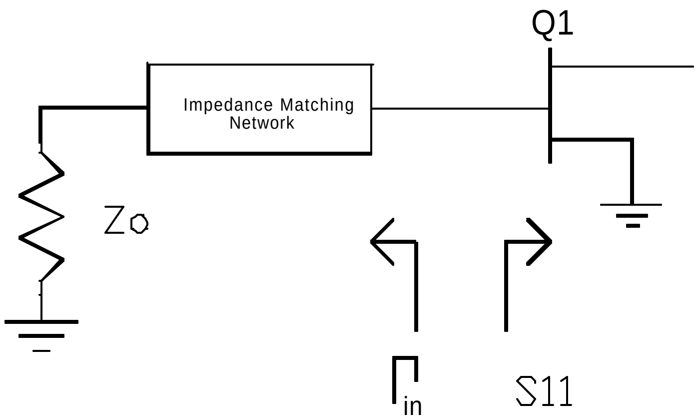
What about Noise Parameters?!??!

G_o (Gamma Opt) is the reflection coefficient of the source impedance presented to the device that allows the device to produce its' f_{min}

Matching circuit losses often limit the ability of the amplifier to achieve a noise figure equivalent to device f_{min}

G_o not necessarily equal to $S11^*$ which means noise match is not equivalent to a gain match

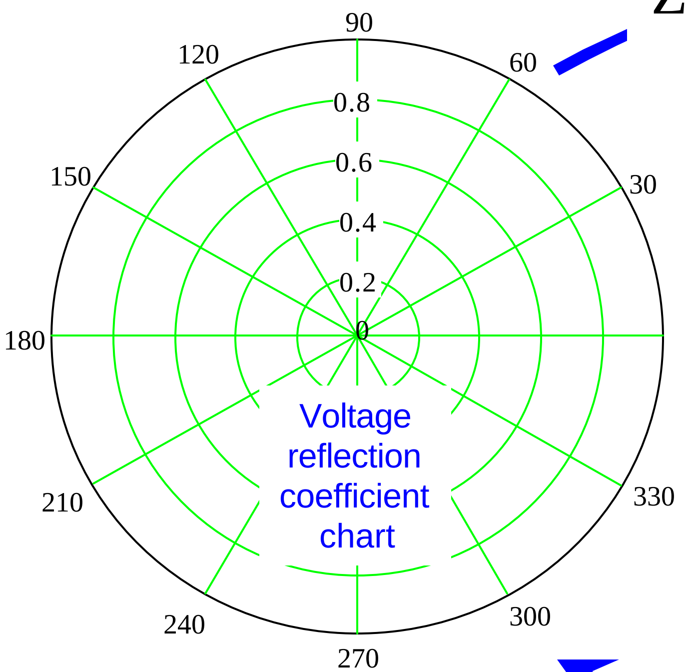
R_n (Noise Resistance) is used to calculate the device's sensitivity in noise figure to changes in source impedance, r_n is normalized to 50 W.

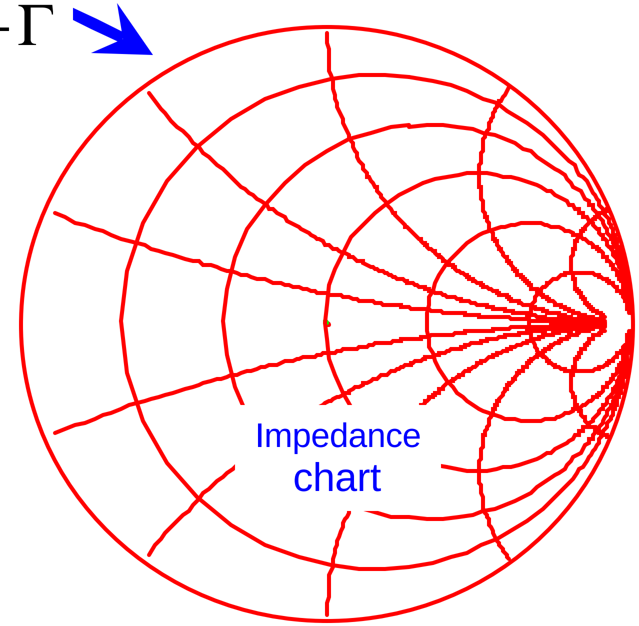


For minimum NF, $\Gamma_{in} = \Gamma_o$
For maximum gain, $\Gamma_{in} = S11^*$

Converting Reflection Coefficients to Impedance with the Smith Chart

$$Z = Z_0 \frac{1+\Gamma}{1-\Gamma}$$





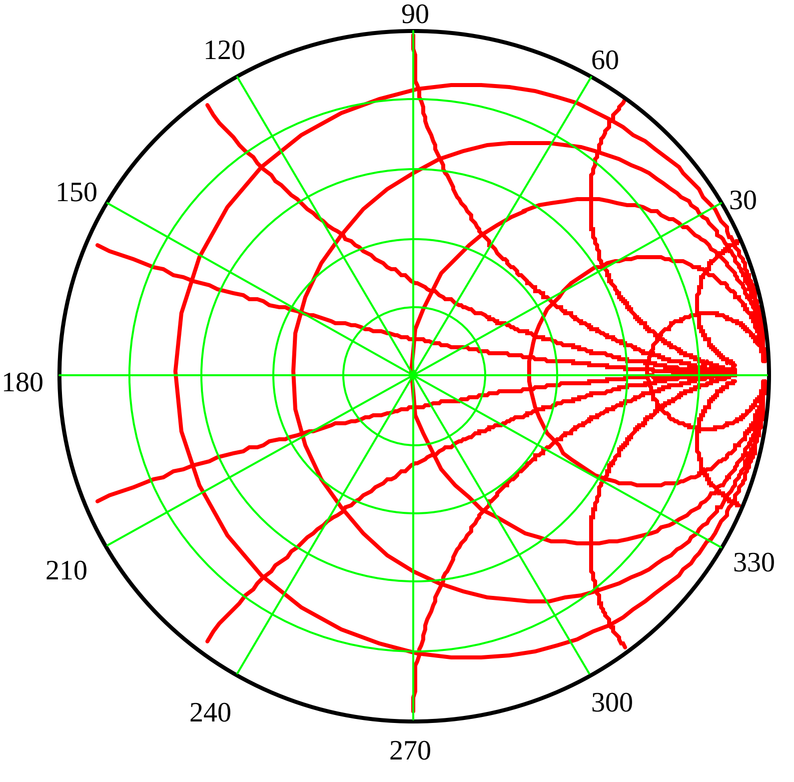
$$\Gamma = \frac{Z - Z_0}{Z + Z_0}$$

The Smith Chart with both Charts Superimposed

Impedance coordinates are shown -- a similar chart exists for admittance coordinates, where

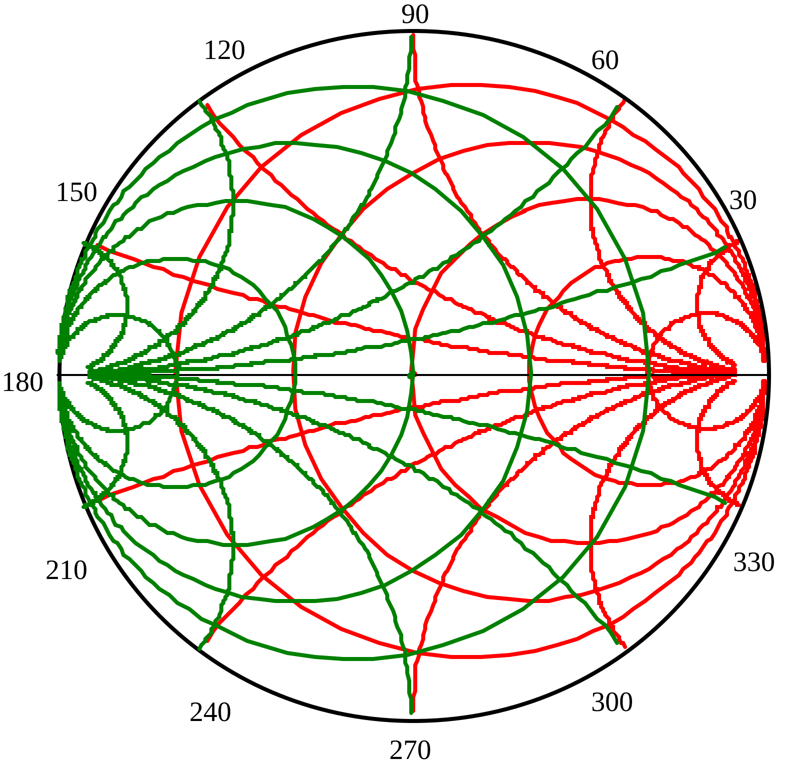
Z = 1/Y

The green polar coordinates are usually left out for clarity. The user substitutes a compass and straightedge.



The Impedance/Admittance Smith chart

When the admittance chart (green coordinates) is overlaid onto the impedance chart (red coordinates), a very useful computing tool is generated.



It chiefly appeals to old timers who are familiar with its use.

Other measures of input characteristics

VSWR = Voltage Standing Wave Ratio

$$\mathrm{VSWR} = \frac{1+|\Gamma|}{1-|\Gamma|}$$

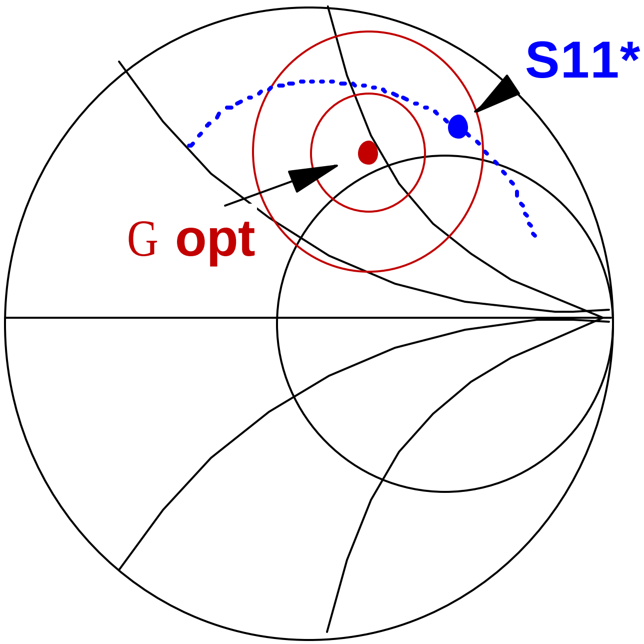
Return Loss

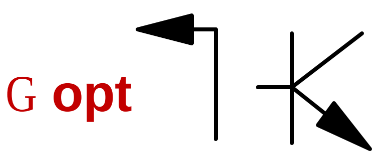
$$\mathrm{RL} = 10\log|\Gamma|^2$$

Mismatch Loss

ML = 10 LOG (1 - G^{2})

Input Impedance Match





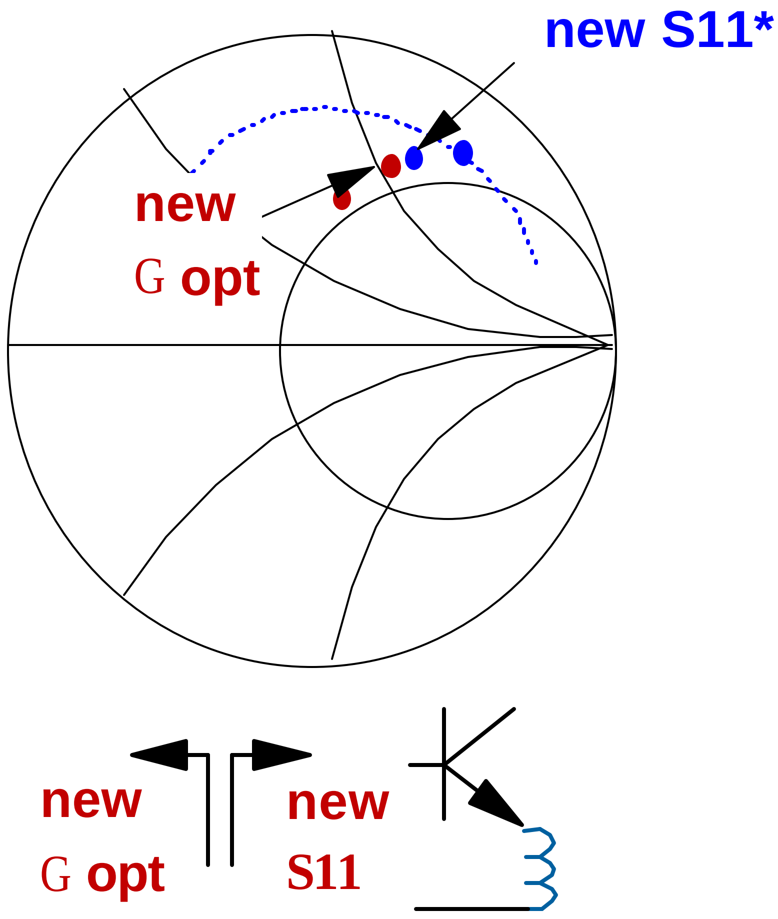
Match to Gopt for minimum noise figure

Noise degrades in circular contours as match moves away from Gopt

Degree of noise degradation is dependent on Rn, the noise resistance

Most amateur applications aim for minimum noise figure and accept input VSWR

Simultaneous Input VSWR and Noise Match

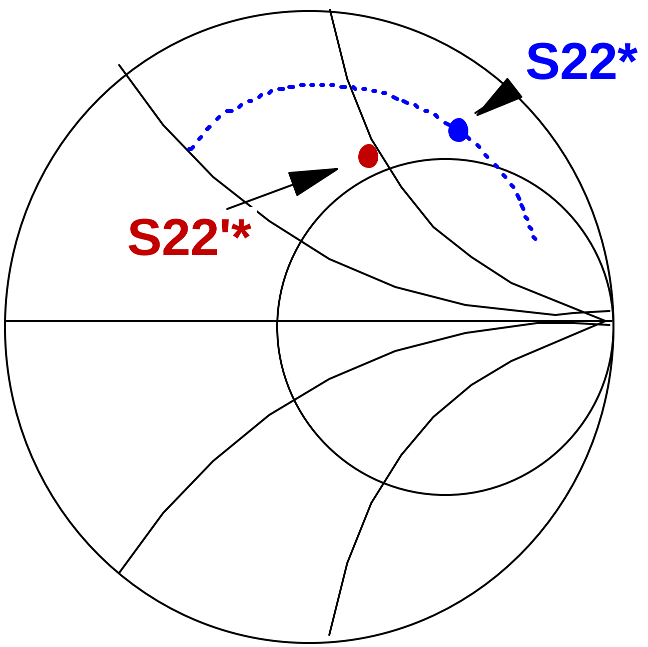


Adding emitter or source inductance rotates Gopt towards S_{11}**

Emitter or source inductance is series feedback which effects gain and stability

Its' effect must be analyzed over as a wide a bandwidth as the device has gain

Output Impedance Match



$$\Gamma_L = \left[S_{22} + \frac{S_{12}\, S_{21}\, \Gamma o}{1 - S_{11}\, \Gamma o} \right]^*$$

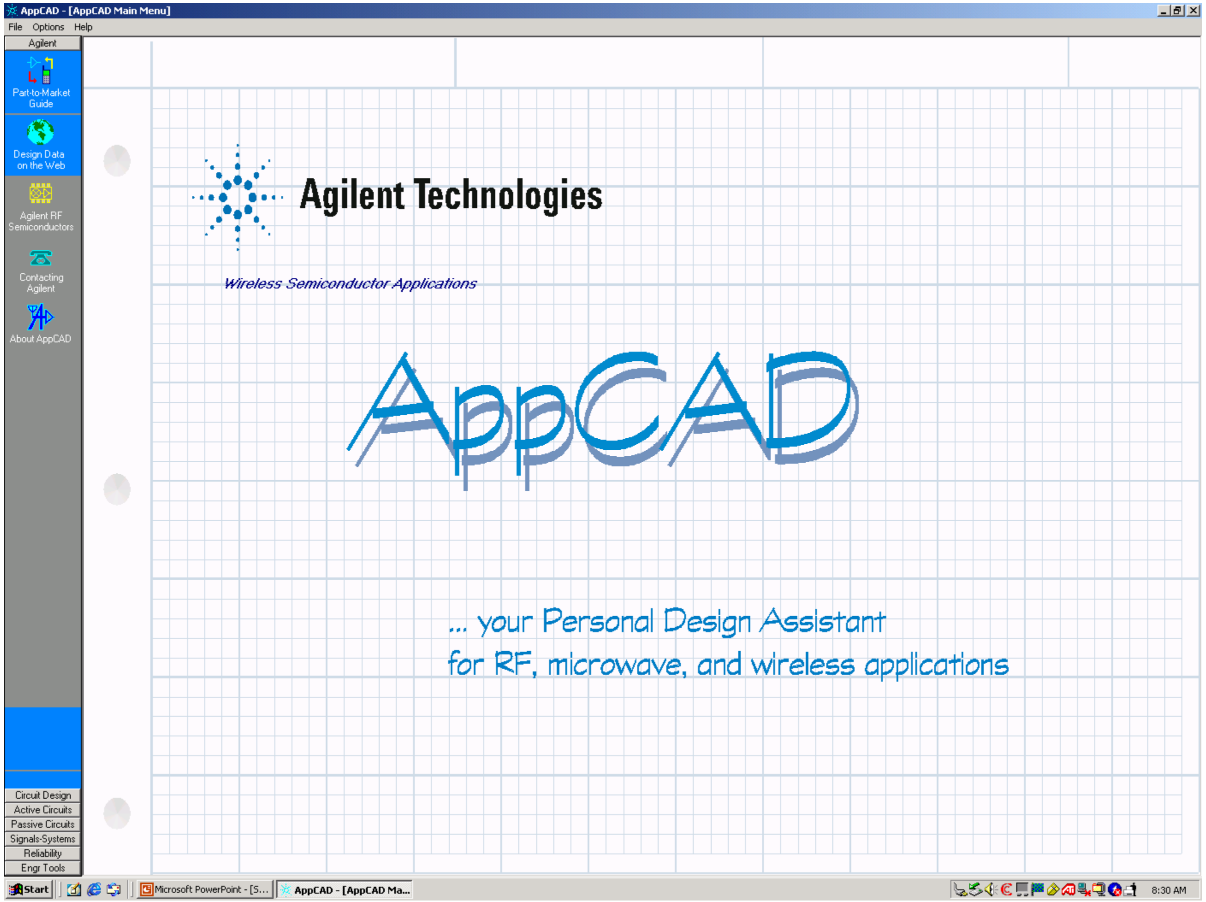
S_{22}'* = G_L is the reflection coefficient of the output matching network with input terminated in Gopt, not 50W

Match to S_{22}'* = G_L for best gain/output VSWR

LNA may not be unconditionally stable when matched for best output VSWR - Some resistive loading may be required to reduce gain to improve stability

Best output VSWR does not necessarily guarantee best P1dB and IP3.

Using AppCAD for Circuit Analysis

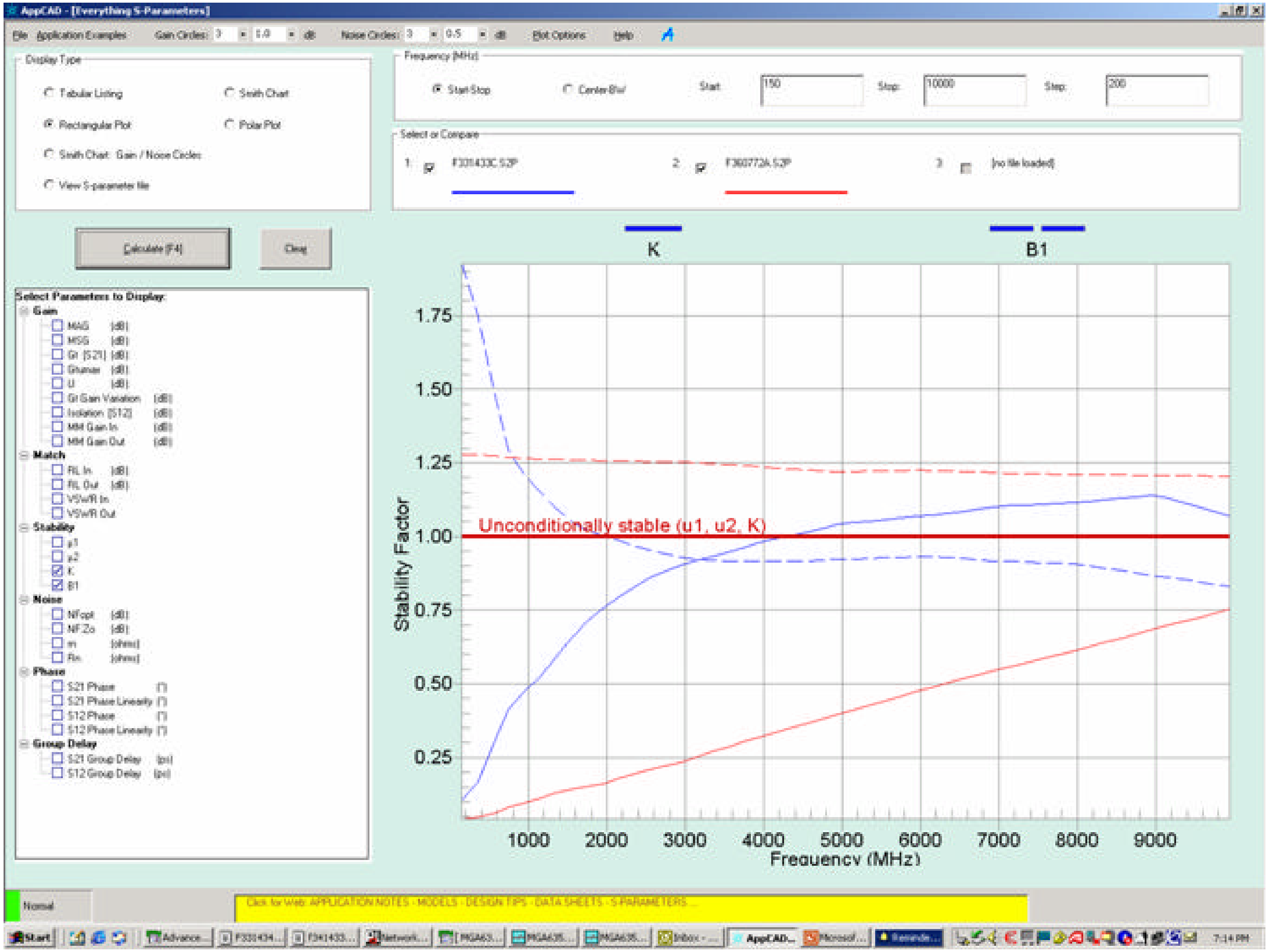


Available for free download at

http://www.semiconductor.agilent.com

http://www.hp.woodshot.com/

ATF-36077 vs ATF-33143
Stability Factors vs Frequency



Stability Factor K calculated from S parameters at each frequency, K>1 for unconditional stability

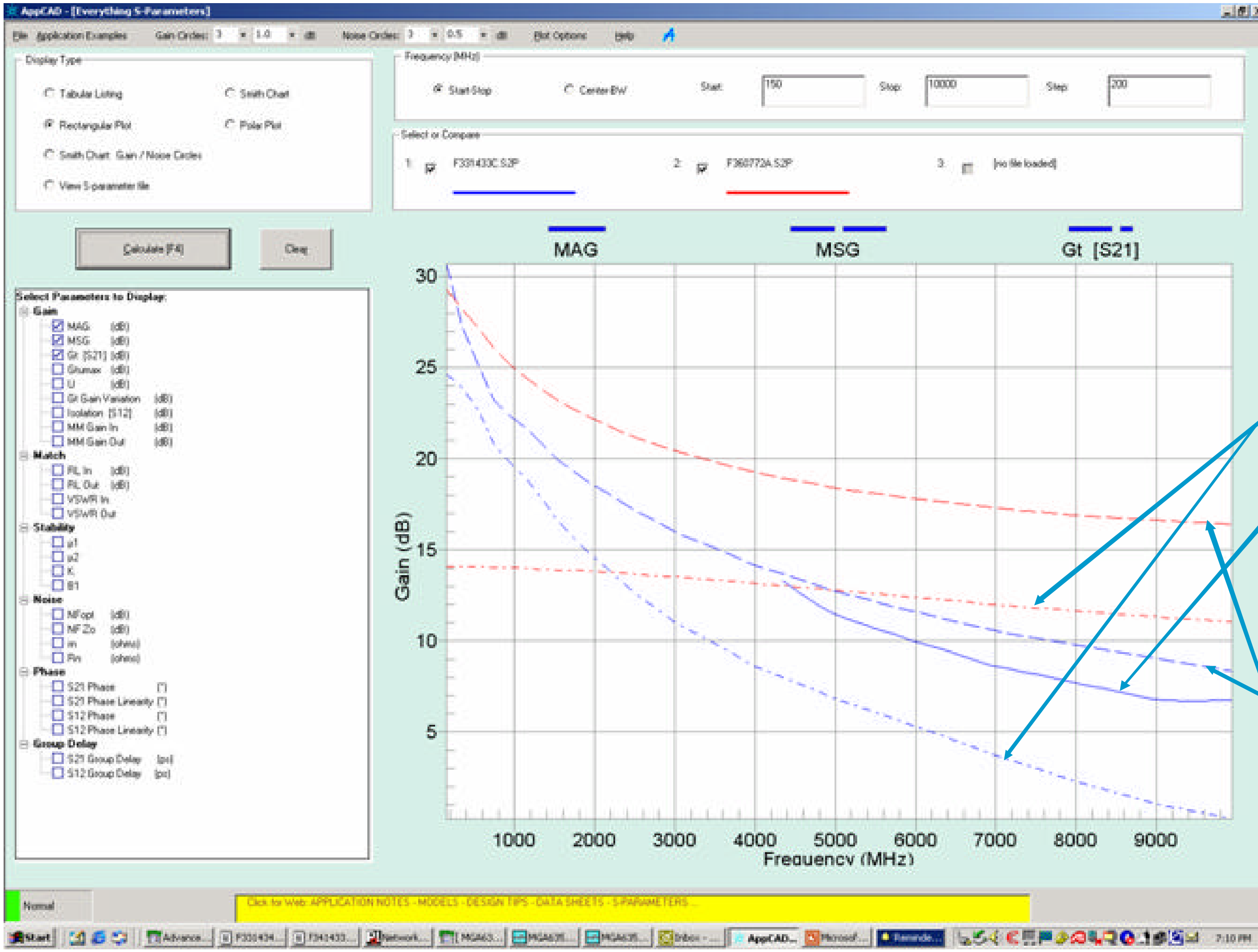
ATF-36077 – K < 1 at all frequencies below 10 GHz

ATF-33143 – K < 1 only below 4.2 GHz, making the device less sensitive to source grounding – better for VHF LNAs

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}||S_{21}|}$$

$$D = S_{11}S_{22} - S_{12}S_{21}$$

ATF-36077 vs ATF-33143
S21 vs MAG vs MSG



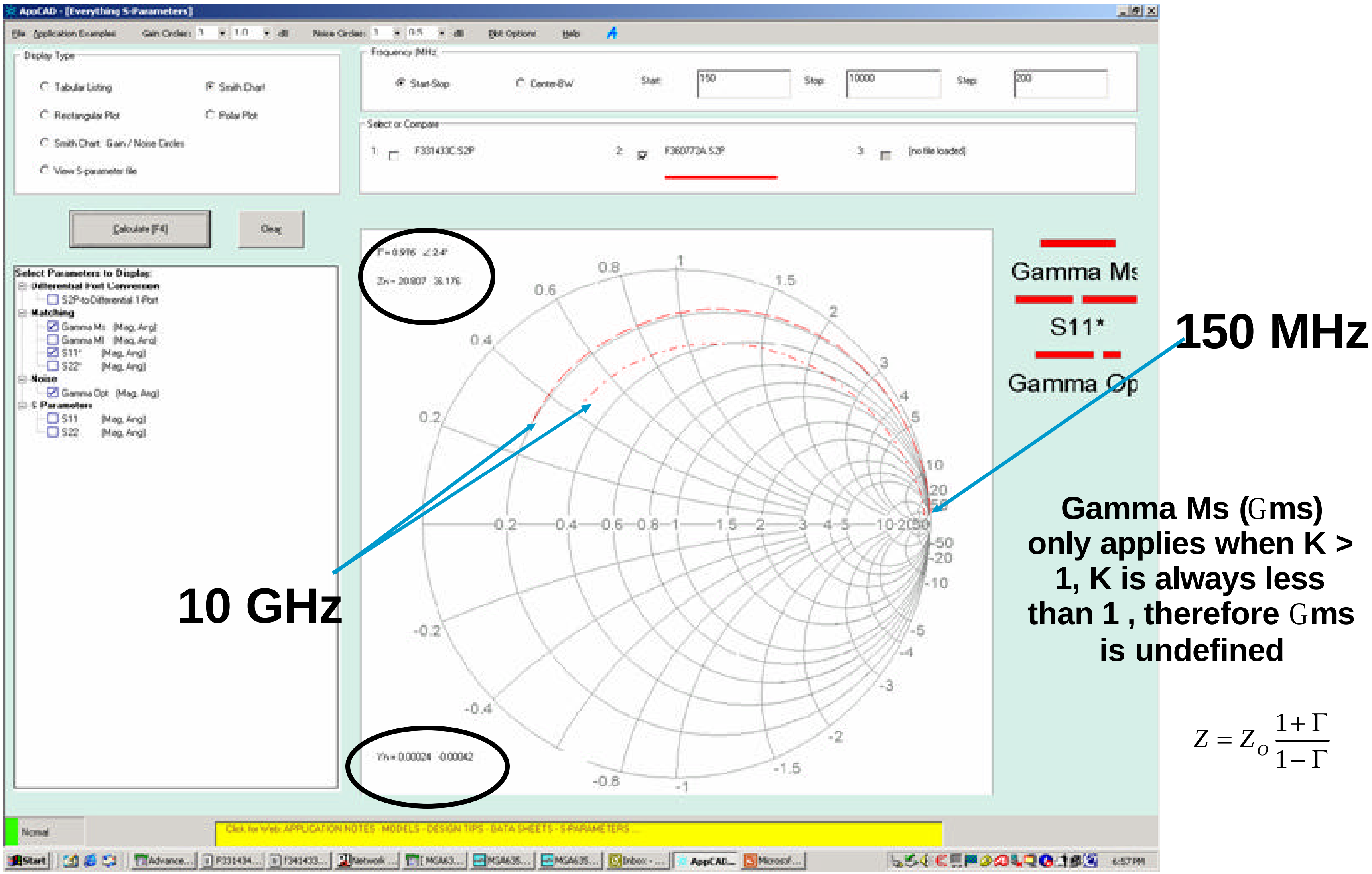
S21 = 50 W Gain

MAG = Maximum Available Gain applies when K>1

MSG = Maximum Stable Gain

Agilent Technologies

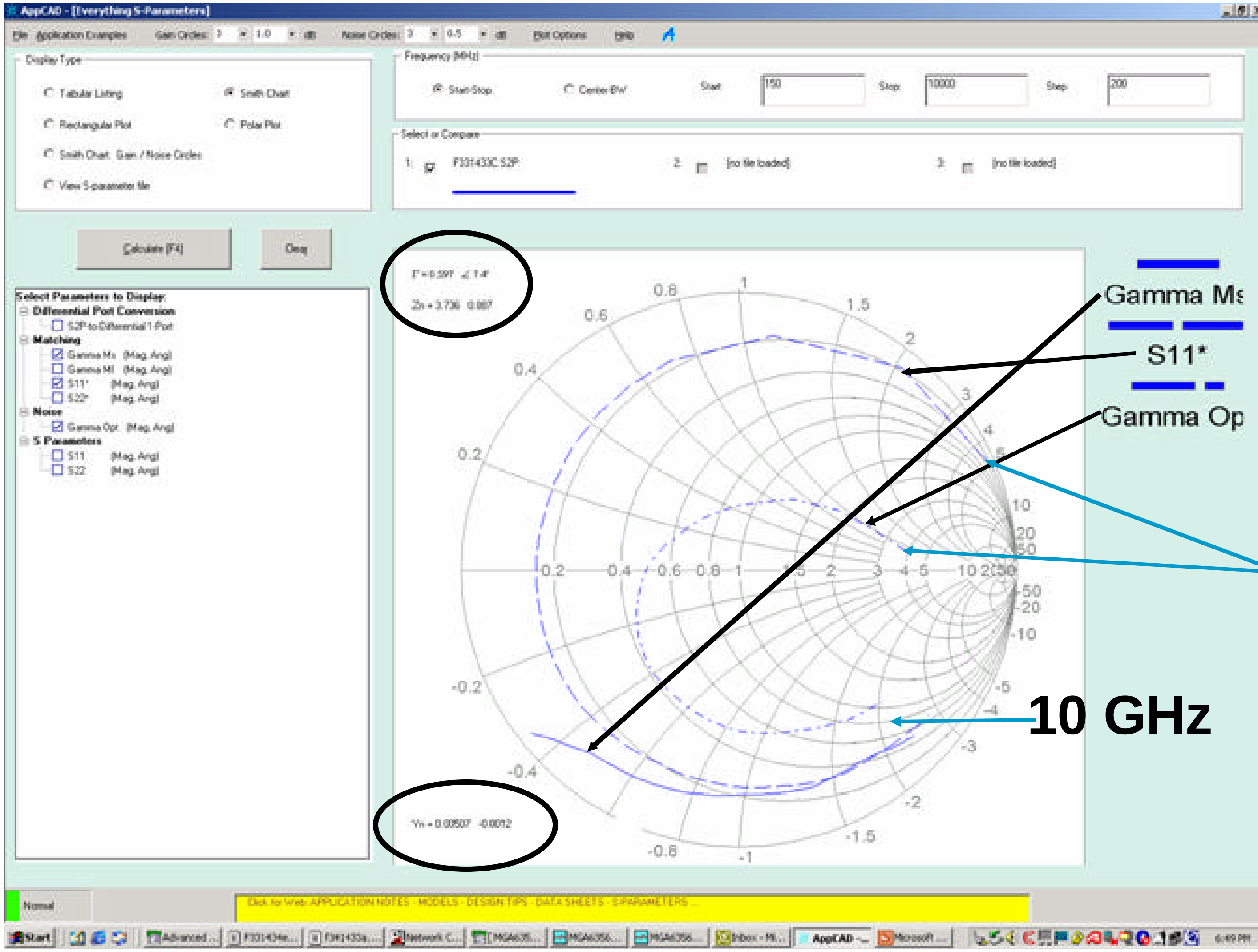
ATF-36077 1.5 V 10 mA
Γo vs S11* vs Γms



Gamma Ms (Γms) only applies when K > 1, K is always less than 1 , therefore Γms is undefined

$$Z = Z_o \frac{1+\Gamma}{1-\Gamma}$$

ATF-33143 3V 60 mA
Go vs S11* vs Gms

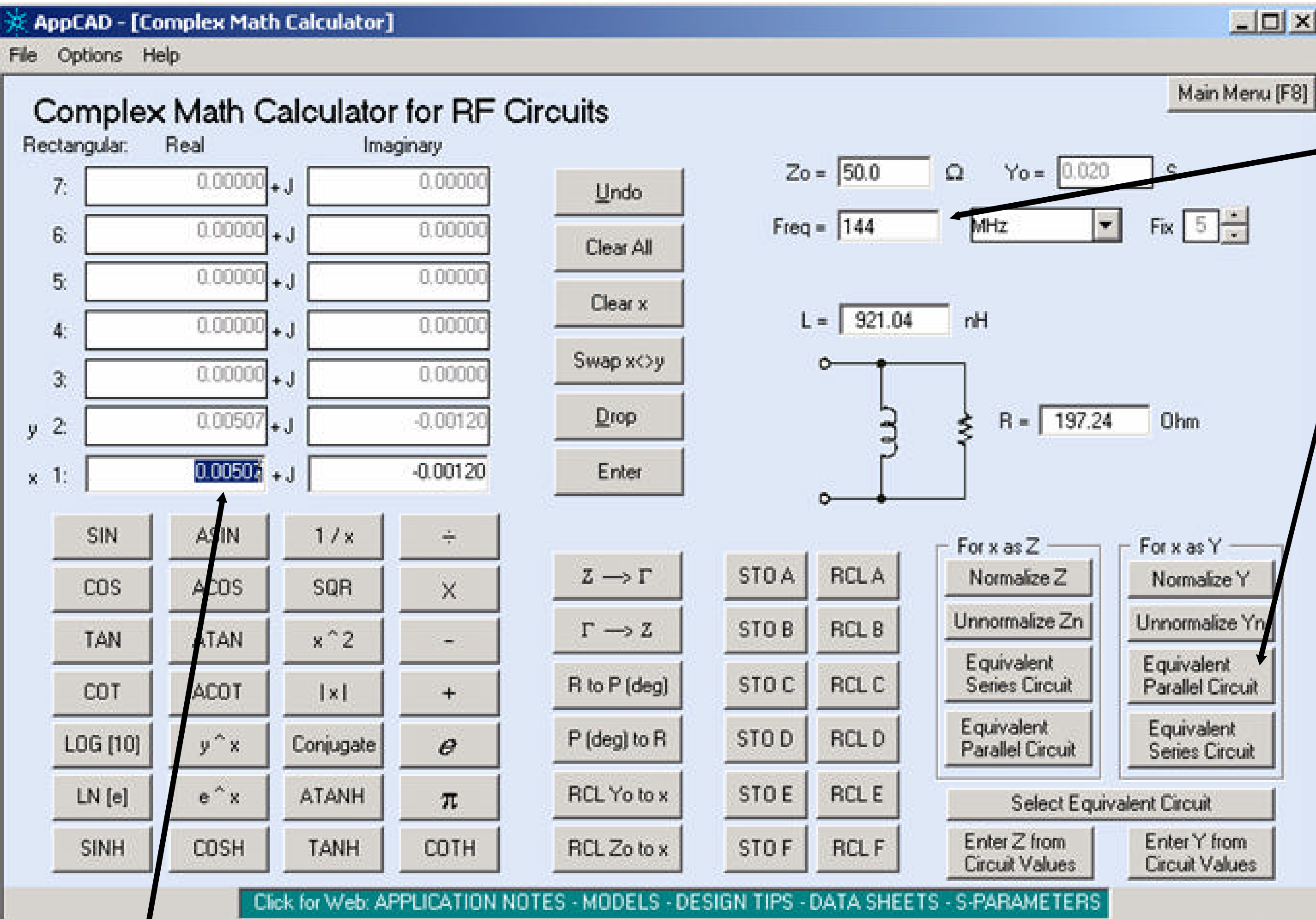


Gamma Ms (Gms) only applies when > 1, K is less than 1 below about 4 GHz therefore Gms undefined belo

4 GHz

$$Z = Z_o \frac{1+\Gamma}{1-\Gamma}$$

Using AppCAD to calculate equivalent circuit that presents Go to the ATF-33143



1. Input Y on Row#1

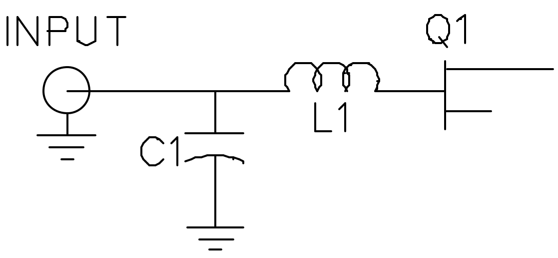
2. Select Frequency

3. Press for equivalent parallel circuit

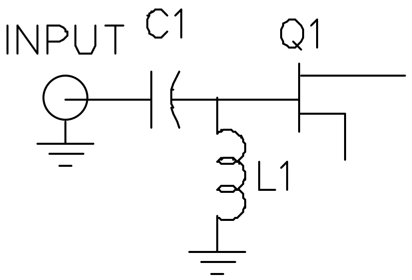
4. Input matching network must transform 50W source impedance to approximately 200W in parallel with 921 nH for the ATF-33143 to produce best NF at 144 MHz

Go expressed as an admittance

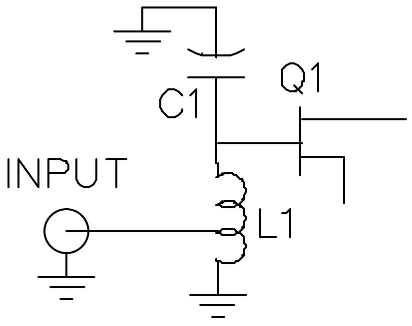
Typical LNA Input Circuits



Low pass network



High pass network

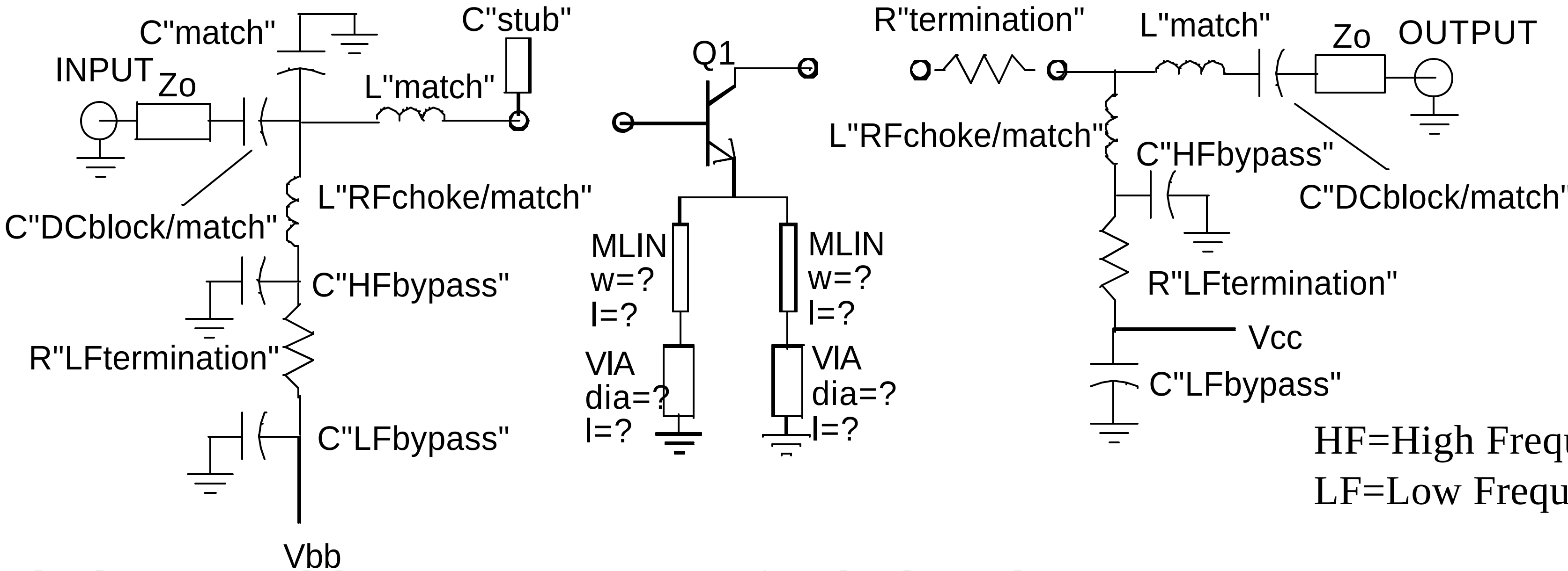


Band pass network

All networks can provide the necessary impedance step-up transformation

Low pass network generally not used at 222 MHz and lower due to poor rejection of out-of-band signals

Integrating Matching Networks and Bias Decoupling Networks



HF=High Frequency
LF=Low Frequency

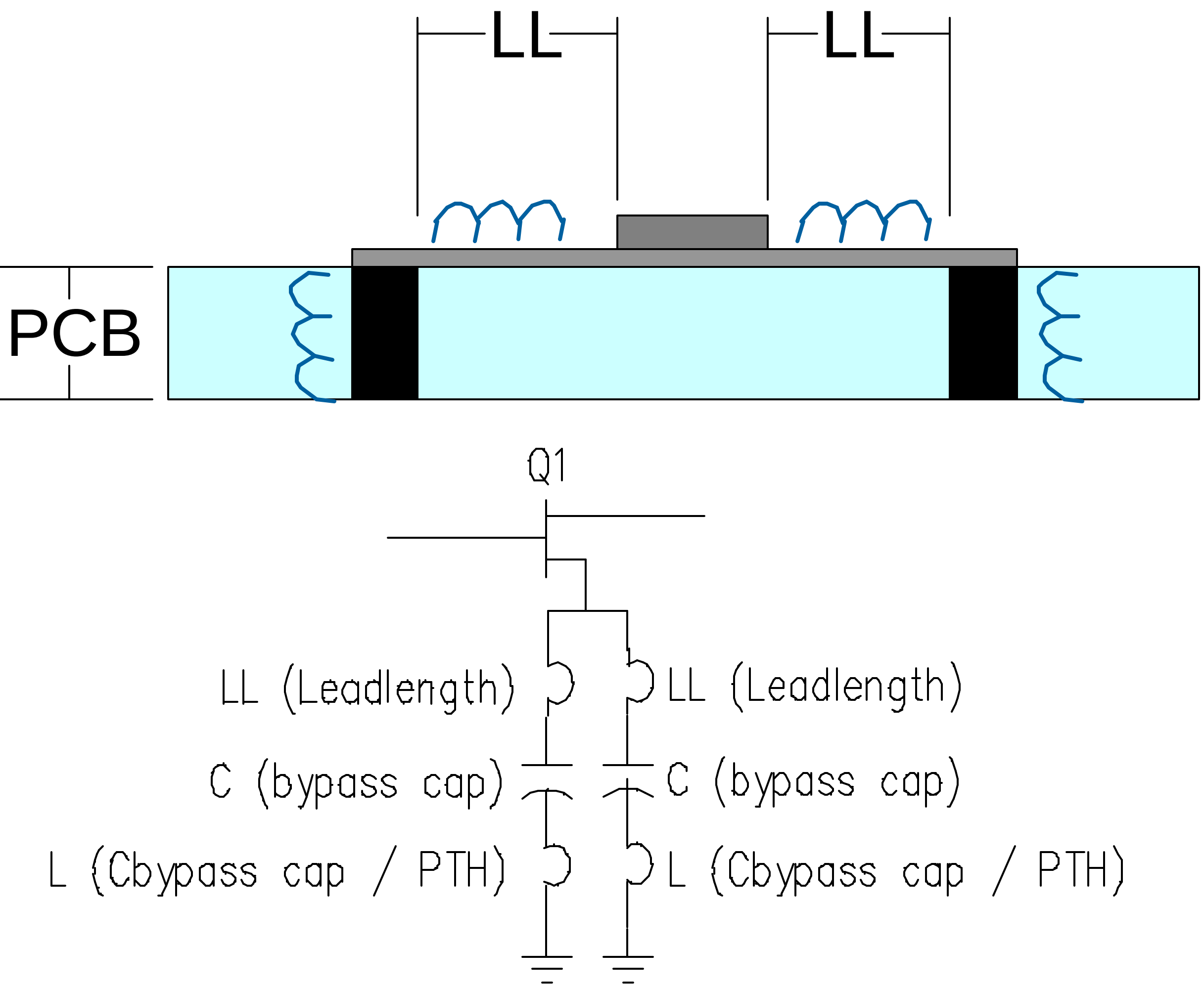
Optimize matching components for in-band performance-NF, Gain, VSWR, Stability

Optimize remaining elements in bias decoupling networks for best out-of-band stability

Retune in-band performance if necessary

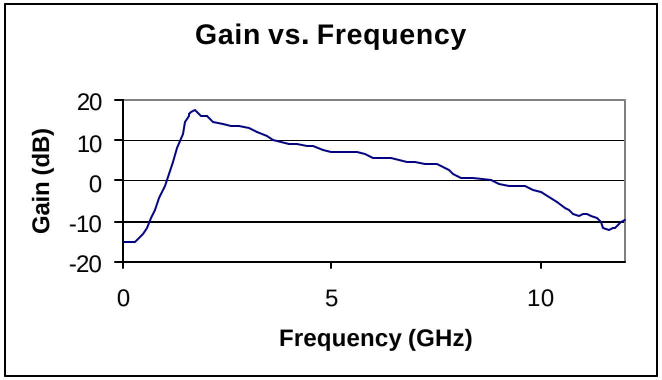
R"termination" (0-27Ω) provides overall stability
R"LFtermination" (50-100Ω) provides stability at F/2 and lower frequency

Contributions to Source Inductance

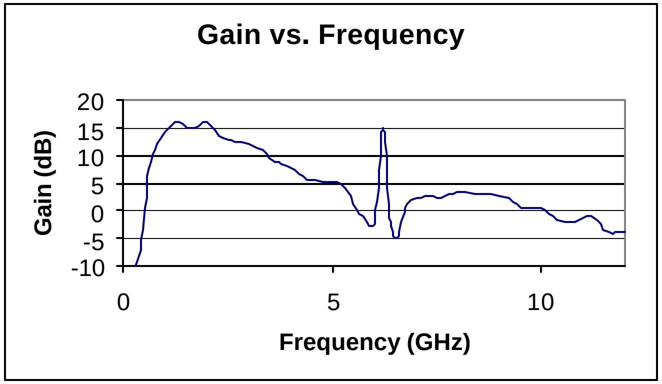


1. Lead length from edge of transistor package to bypass cap or plated through hole adds inductance
2. Use of a source resistor bypass capacitor can alter circuit stability
3. The inductance associated with the bypass capacitor and the equivalent inductance due to the thickness of printed circuit board

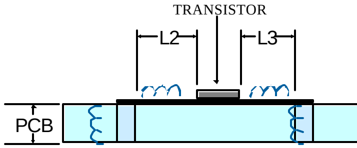
Effect of Source Inductance on Amplifier Performance

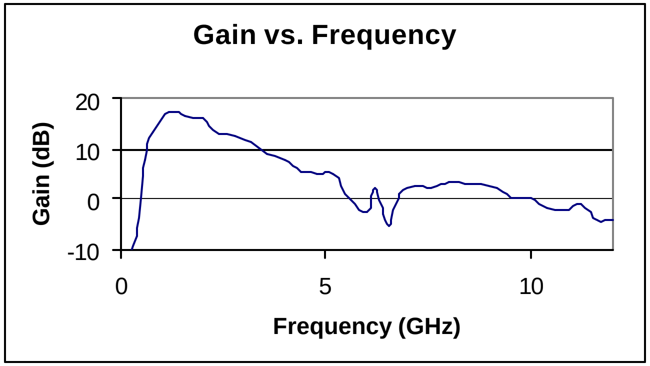


Minimal source inductance



Excessive and unacceptable amount of source inductance





Moderate but acceptable source inductance

Source inductance is a convenient way to improve S11 and reduce gain which will improve IIP3 however…. Excessive source inductance causes out-of-band gain peaking and resultant instabilities and oscillations

Low Noise Amplifier for 144 MHz using the ATF-33143 PHEMT designed by WD5AGO

ATF-33143 S Parameters with low frequency prediction

!ATF-33143
!s-parameters at Vds=3V, Id=60mA. Last updated 25/02/02 AR.
!Data below 500 MHz extrapolated based on non-linear model prediction

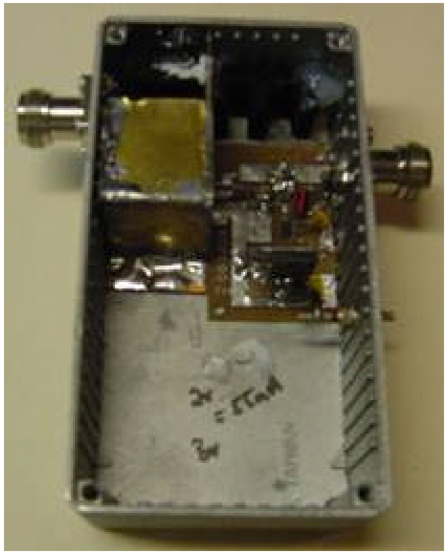
!Freq(GHz)	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
# ghz s ma r 50								
0.1	0.97	-15	16.5	165.0	0.010	80.0	0.07	-106
0.3	0.93	-44	15.3	146	0.027	67	0.18	-114
0.5	0.87	-75.3	14.06	133	0.039	55.1	0.27	-124.2
0.8	0.78	-114.7	10.26	110	0.055	42.6	0.36	-153.9
1	0.77	-122.3	9.56	105.5	0.057	40.5	0.37	-158.8
1.5	0.74	-151.6	6.91	87.6	0.068	33.5	0.41	-178.7
1.8	0.73	-164.6	5.87	79.3	0.072	30.8	0.43	172.6
2	0.73	-171.8	5.3	74.4	0.075	29	0.44	167.5
2.5	0.73	171	4.27	62.8	0.082	25.1	0.47	158.5
3	0.74	158.1	3.54	53.1	0.089	21.4	0.5	151
4	0.75	136.4	2.68	35.4	0.103	13.2	0.52	138.6
5	0.75	116.9	2.19	17.7	0.117	2.8	0.52	124.4
6	0.77	97.8	1.84	-0.6	0.128	-9.7	0.53	107.8
7	0.79	79.9	1.53	-18.6	0.135	-23.2	0.56	90.2
8	0.82	64.5	1.3	-34.4	0.137	-34.6	0.59	74.7
9	0.83	50.4	1.13	-48.5	0.141	-44.5	0.62	62.7
10	0.86	36.4	1.02	-63.5	0.15	-56.2	0.65	50.9
11	0.88	21.6	0.9	-79.5	0.151	-69.4	0.68	37.4
12	0.9	7.3	0.78	-95.1	0.146	-82.1	0.71	21.4
13	0.91	-5	0.66	-109.7	0.137	-94	0.74	5.8
14	0.91	-15.5	0.57	-121.4	0.13	-102.7	0.77	-6.1
15	0.92	-27.5	0.51	-133.9	0.128	-112.4	0.8	-15.8
16	0.93	-40.6	0.46	-146.6	0.13	-123	0.82	-25.8
17	0.94	-52.3	0.42	-160.3	0.127	-135.3	0.82	-37.9
18	0.93	-61.4	0.36	-170.9	0.117	-144	0.84	-49.7

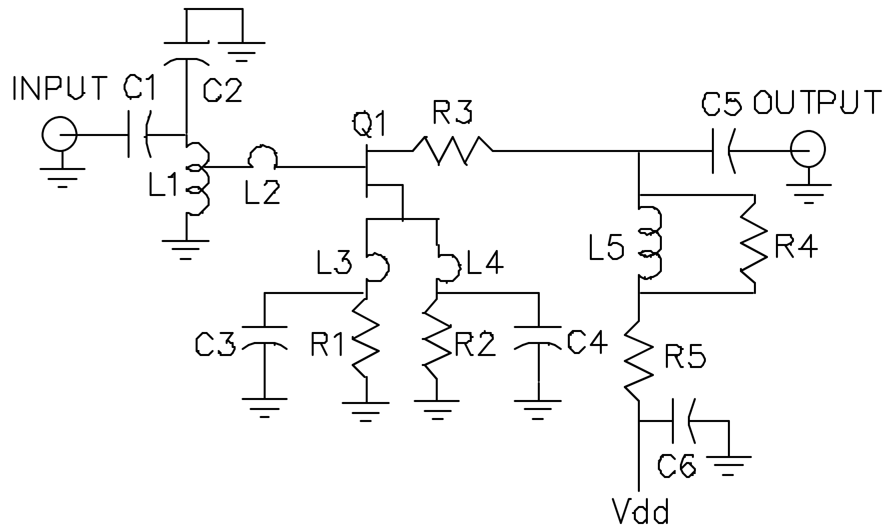
ATF-33143 Noise Parameters with low frequency prediction

!noise parameters at Vds=3V, Id=60mA
! Freq FMIN GAMMA OPT Rn
! (GHz) (dB) Mag Ang 50 Ohm

0.1	0.23	0.62	5	0.060
0.2	0.23	0.58	9	0.059
0.3	0.23	0.53	15	0.058
0.4	0.23	0.48	19	0.058
0.5	0.23	0.43	29.20	0.06
0.9	0.28	0.35	42.40	0.06
1.0	0.29	0.35	45.00	0.07
1.5	0.34	0.26	68.80	0.06
1.8	0.34	0.23	93.30	0.04
2.0	0.38	0.22	109.70	0.05
2.5	0.52	0.25	150.60	0.03
3.0	0.53	0.30	167.50	0.03
4.0	0.61	0.39	-160.30	0.04
5.0	0.68	0.47	-134.70	0.06
6.0	0.83	0.52	-112.10	0.11
7.0	0.91	0.58	-89.70	0.22
8.0	1.04	0.61	-71.50	0.36
9.0	1.09	0.66	-54.80	0.56
10.0	1.13	0.70	-41.40	0.73

Schematic for the WD5AGO ATF-33143 144 MHz LNA

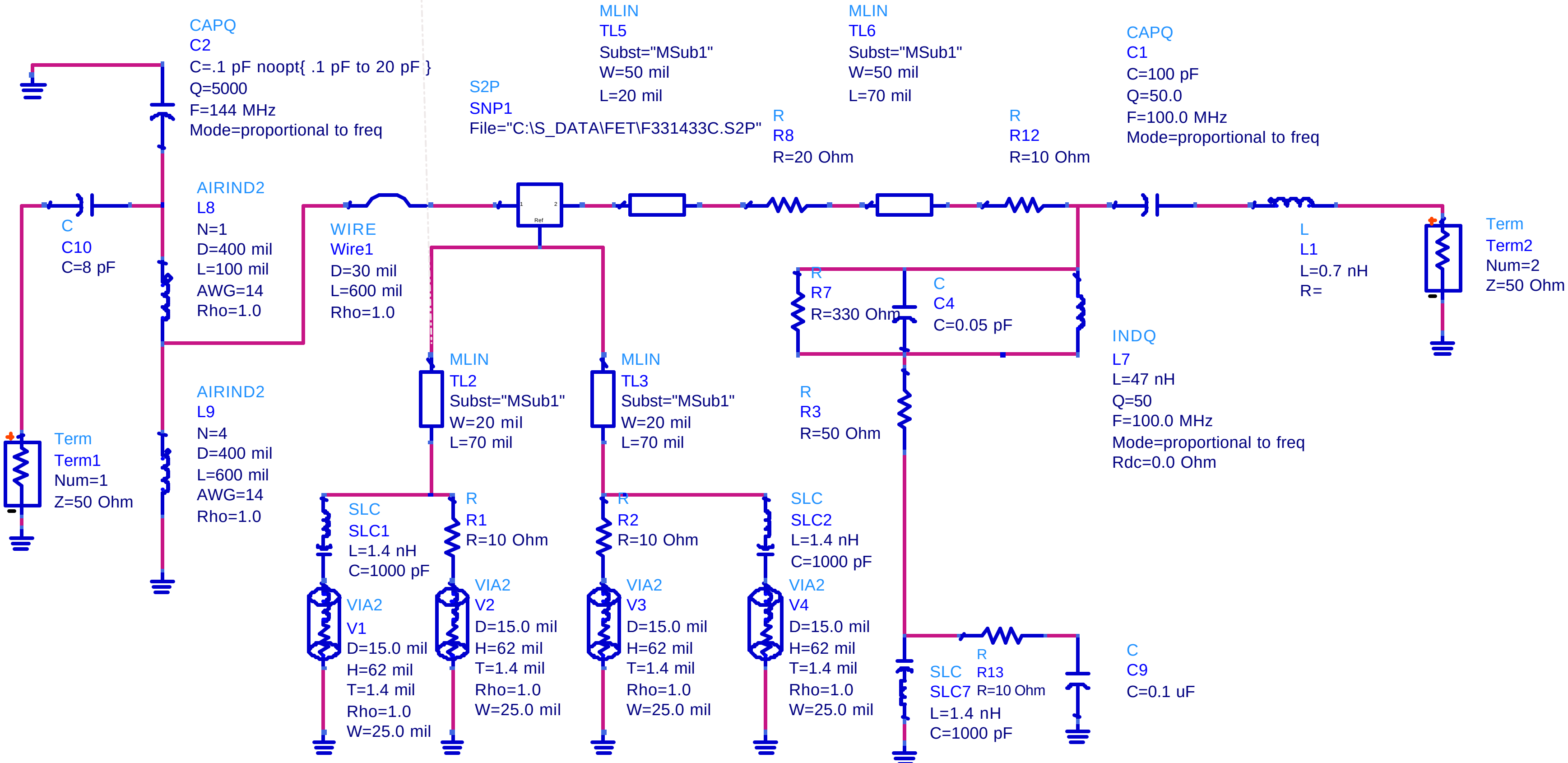




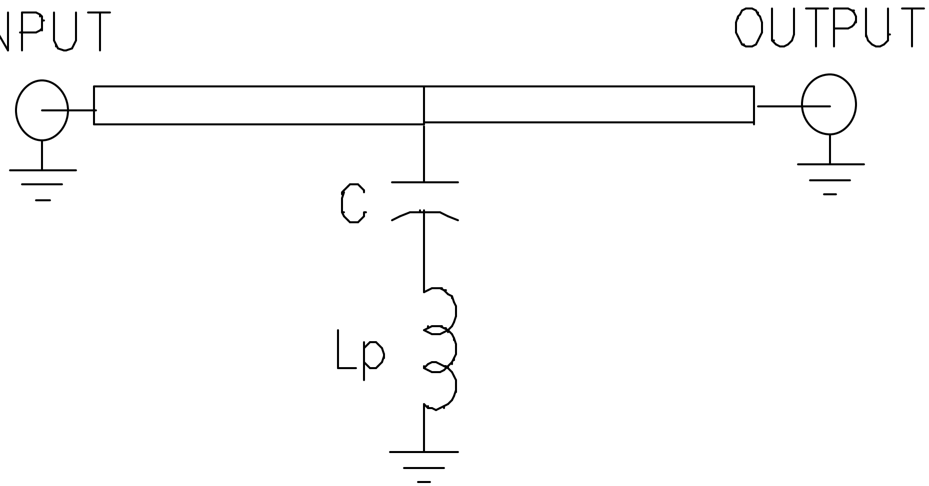
Vds=3V
Id=60 mA

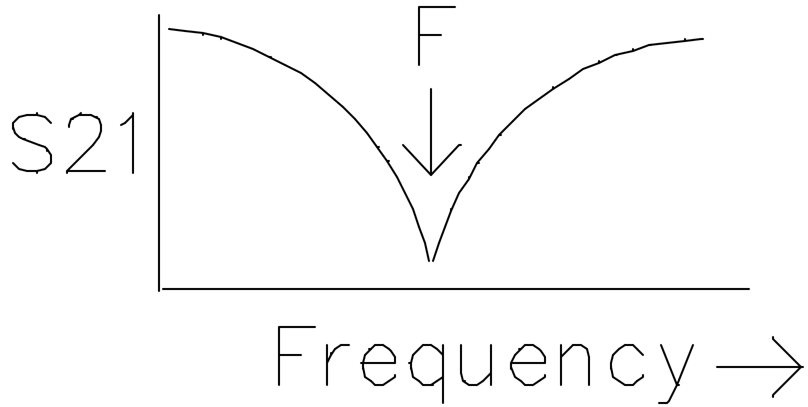
C1,C2	0.8 to 10 pF Johansen variable capacitor
C3,C4	1000 pF chip capacitor
C5	100 pF chip capacitor
C6	0.1 uF chip capacitor
L1	5 Turns #14 guage 0.4” dia. c to c spaced wire diameter tap 1 T from top enclosed in a 0.75” by 1” brass enclosure
L2	0.6” length wire 0.030” diameter
L3,L4	0.050” wide by 0.080” length etch between Q1 and C3,C4
L5	47 nH chip inductor
Q1	Agilent ATF-33143 PHEMT
R1,R2	15 Ω chip resistor
R3	27 Ω chip resistor
R4	330 Ω chip resistor
R5	50 Ω chip resistor

ADS Simulation for the WD5AGO ATF-33143 144 MHz LNA



Chip Capacitor Parasitics - A First Approximation



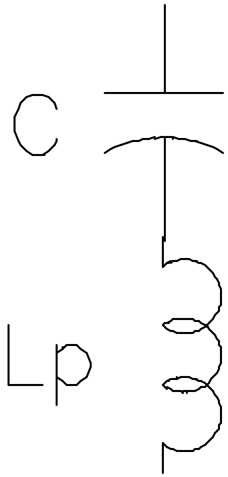


A capacitor shunted across a microstripline exhibits a first order series resonance at a frequency where the capacitance C and its' associated parasitic lead inductance Lp resonate. The effect is shown as a reduction in S21 at frequency F

OR

Lp can then be easily calculated by $\omega = 2 \pi F = 1/ \text{SQRT} (L C)$

Chip Capacitor Parasitics - A First Approximation



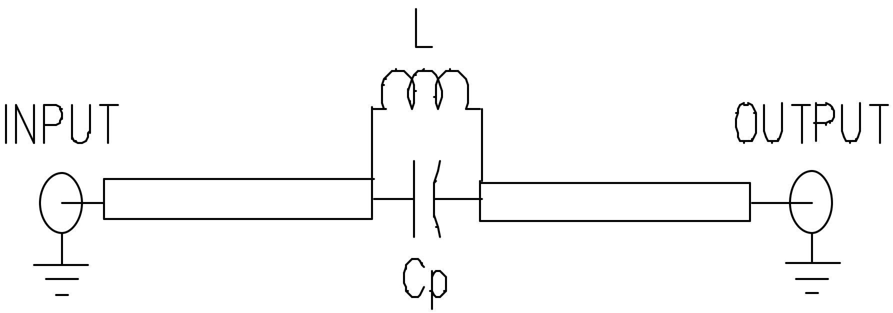
Capacitor (pF)	Associated Inductance Lp
1	0.71
8.2	0.78
27	0.79
1000	1.2

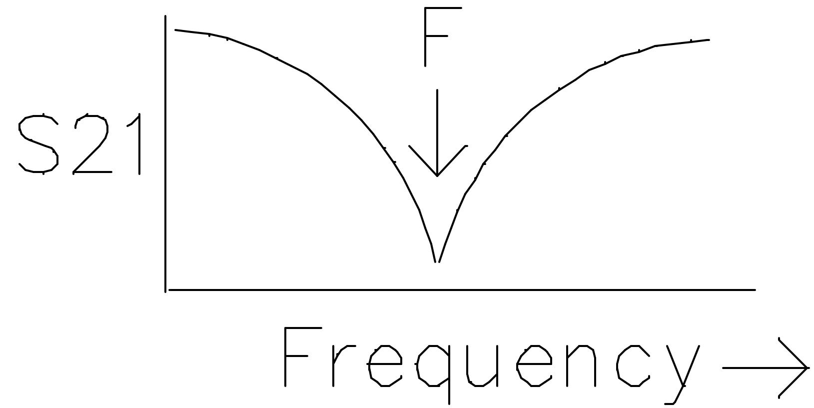
Sample data

Capacitors are ATC 0.050” square ceramic

Parasitic inductance should be included in circuit designs for best correlation between simulation and actual bench performance

Chip Inductor Parasitics - A First Approximation

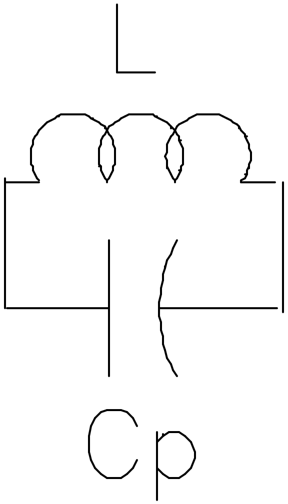




An inductor inserted in series with a microstripline exhibits a first order parallel resonance at a frequency where the inductor L and its' associated shunt parasitic capacitance Cp resonate. The effect is shown as a reduction in S21 at frequency F OR

Lp can then be easily calculated by w= 2 p F = 1/ SQRT (L C)

Chip Inductor Parasitics - A First Approximation



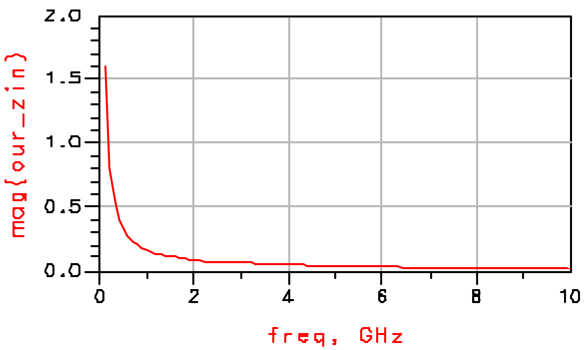
Inductor (nH)	Associated shunt capacitance Cp
4	0.048
10	0.076
27	0.170
560	0.128

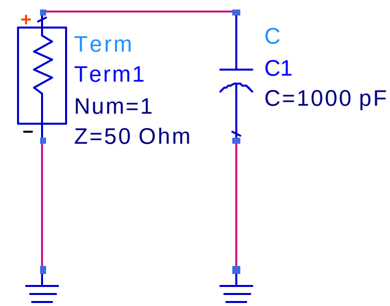
Sample data

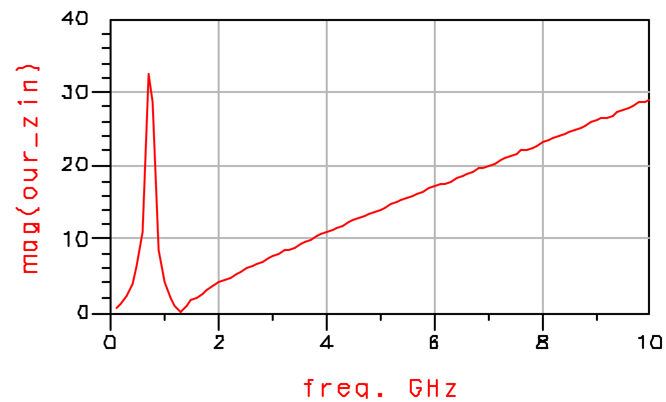
Inductors are Coilcraft 1008CS style

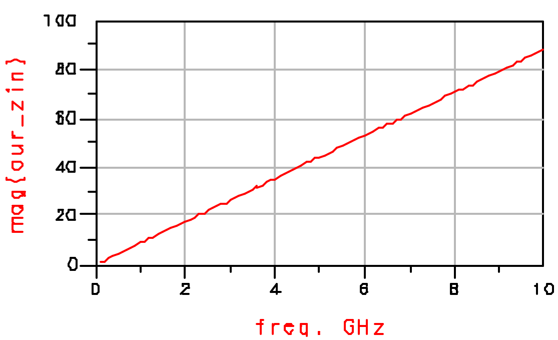
Parasitic shunt capacitance should be included in circuit designs for best correlation between simulation and actual bench performance

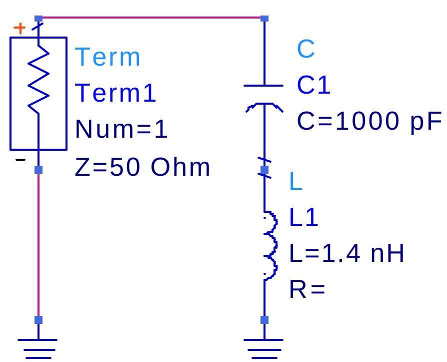
Effect of paralleling two capacitors of different values

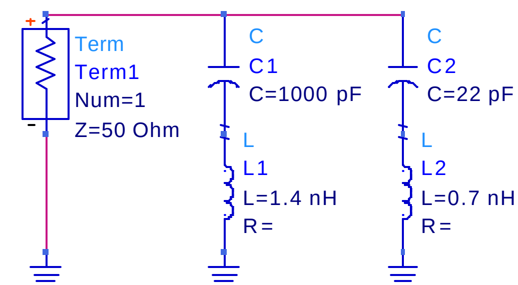








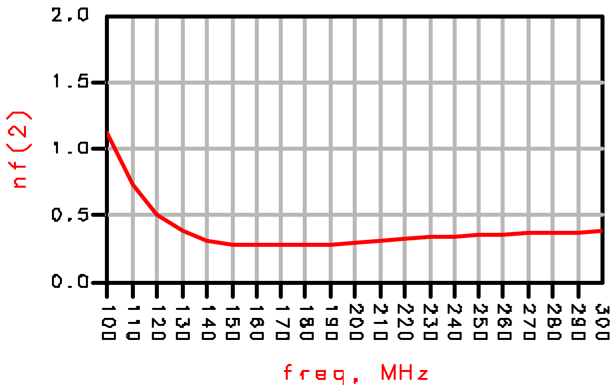




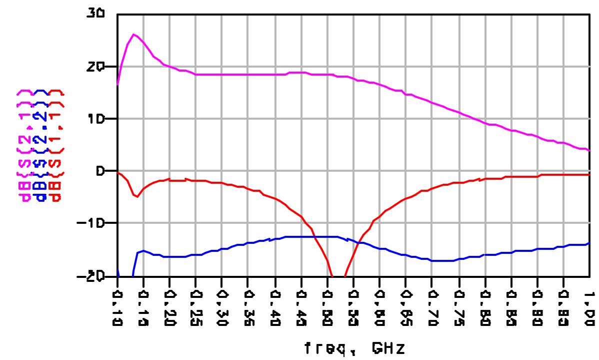
Paralleling 2 caps of equal C and L cuts Z in half at all freq

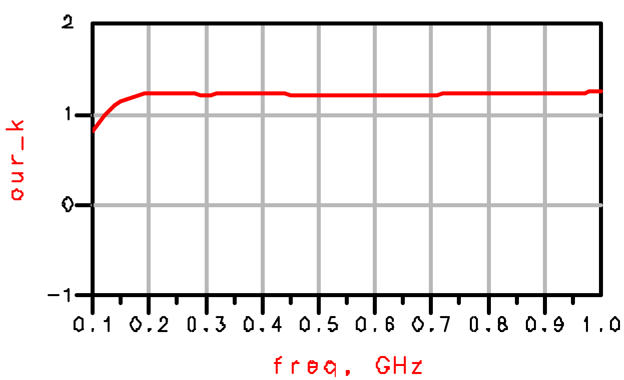
Paralleling 22 pF cap with 1000 pF cap may lower Z at 1.2 GHz, however, Z at 0.8 GHz increases dramatically

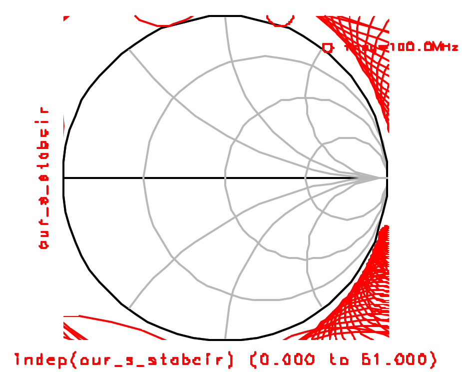
ADS Simulated Performance for the WD5AGO ATF-33143 144 MHz LNA



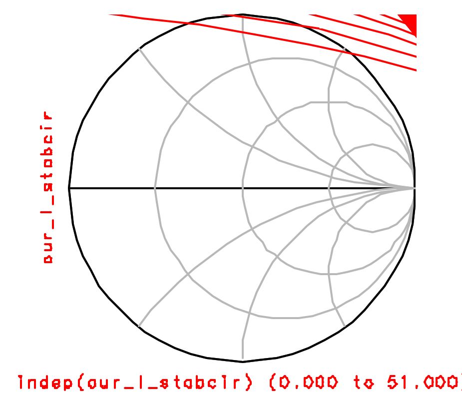
Measured
S21=27 dB
S11 = -4.4 dB
S22=-11 dB
NF=0.27 dB







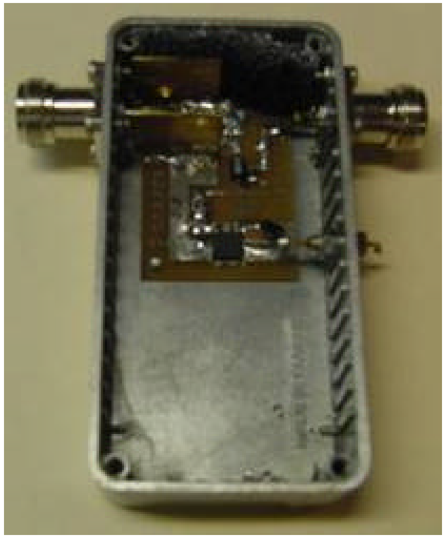
Input Stability Circle

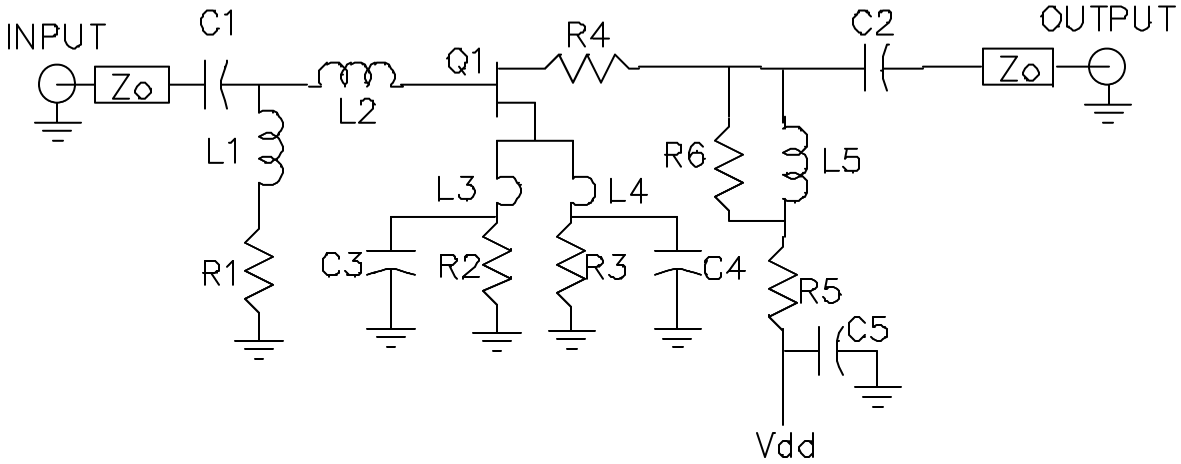


Output Stability Circle

Low Noise Amplifier for 432 MHz using the ATF-33143 PHEMT designed by WD5AGO

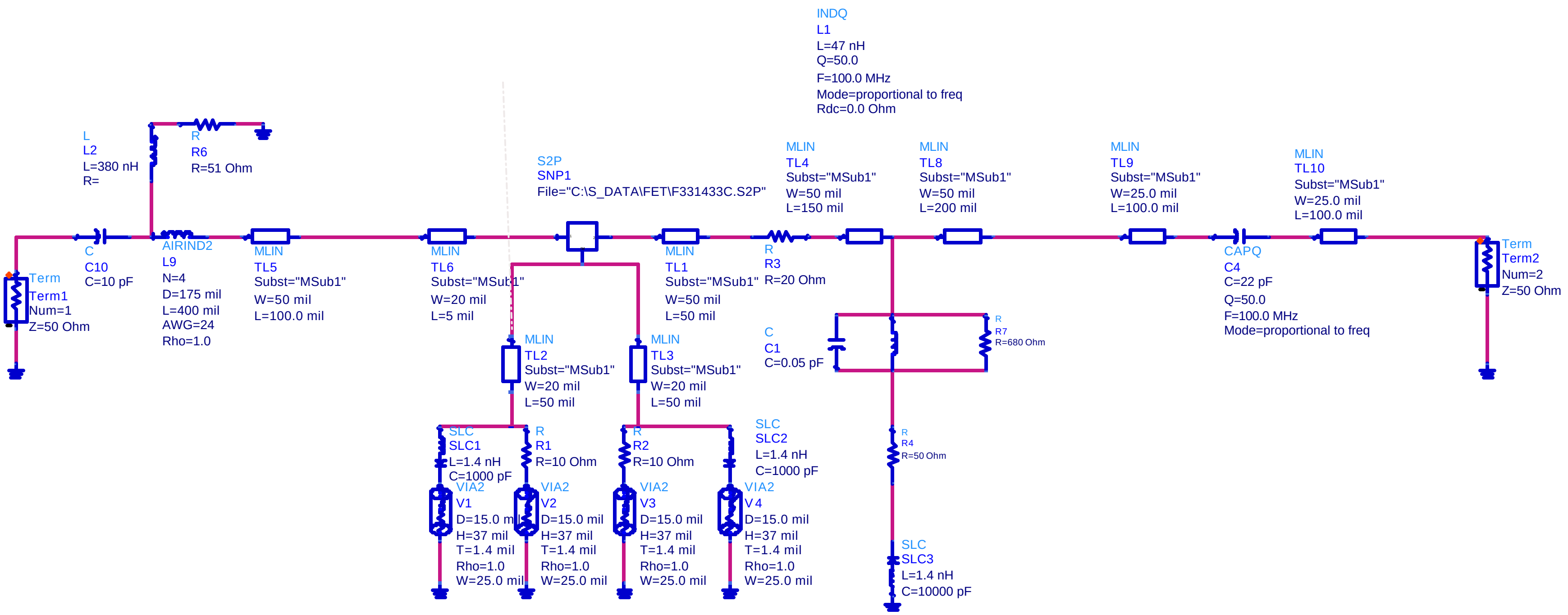
WD5AGO ATF-33143 432 MHz LNA



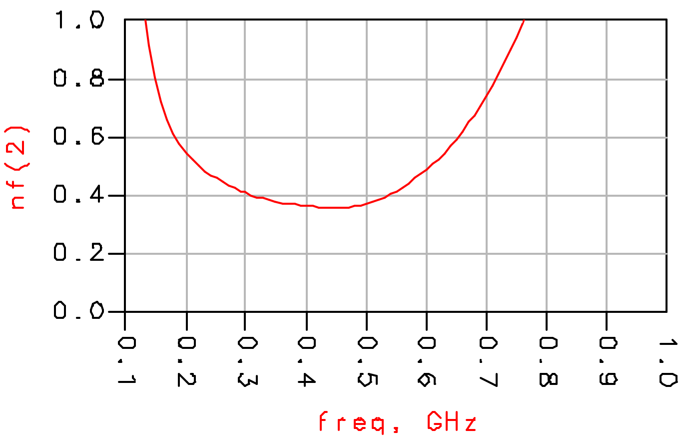


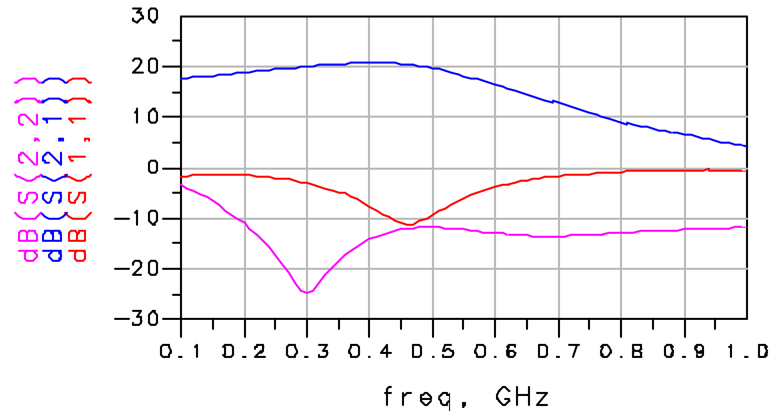
C1	10 pF chip capacitor
C2	50 pF chip capacitor
C3,C4	1000 pF chip capacitor
C5	0.01 uF chip capacitor
L1	380 nH chip inductor
L2	Airwound inductor 4 turns #24 guage wire 0.175”ID, 0.4” length
L3,L4	Microstrip 0.020” wide by 0.050” in length
L5	100 nH chip inductor
Q1	Agilent ATF-33143 PHEMT
R1	51 Ω chip resistor
R2,R3	10 Ω chip resistor
R4	20 Ω chip resistor – adjust for stability
R5	50 Ω chip resistor
R6	680 Ω chip resistor

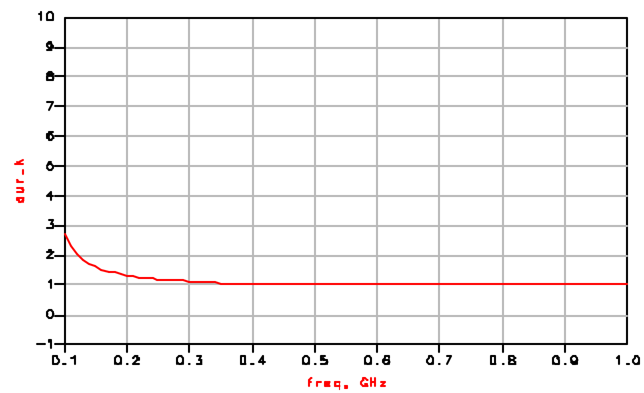
ADS Simulation of the WD5AGO ATF-33143 432 MHz LNA



ADS Simulated Performance for the WD5AGO ATF-33143 432 MHz LNA







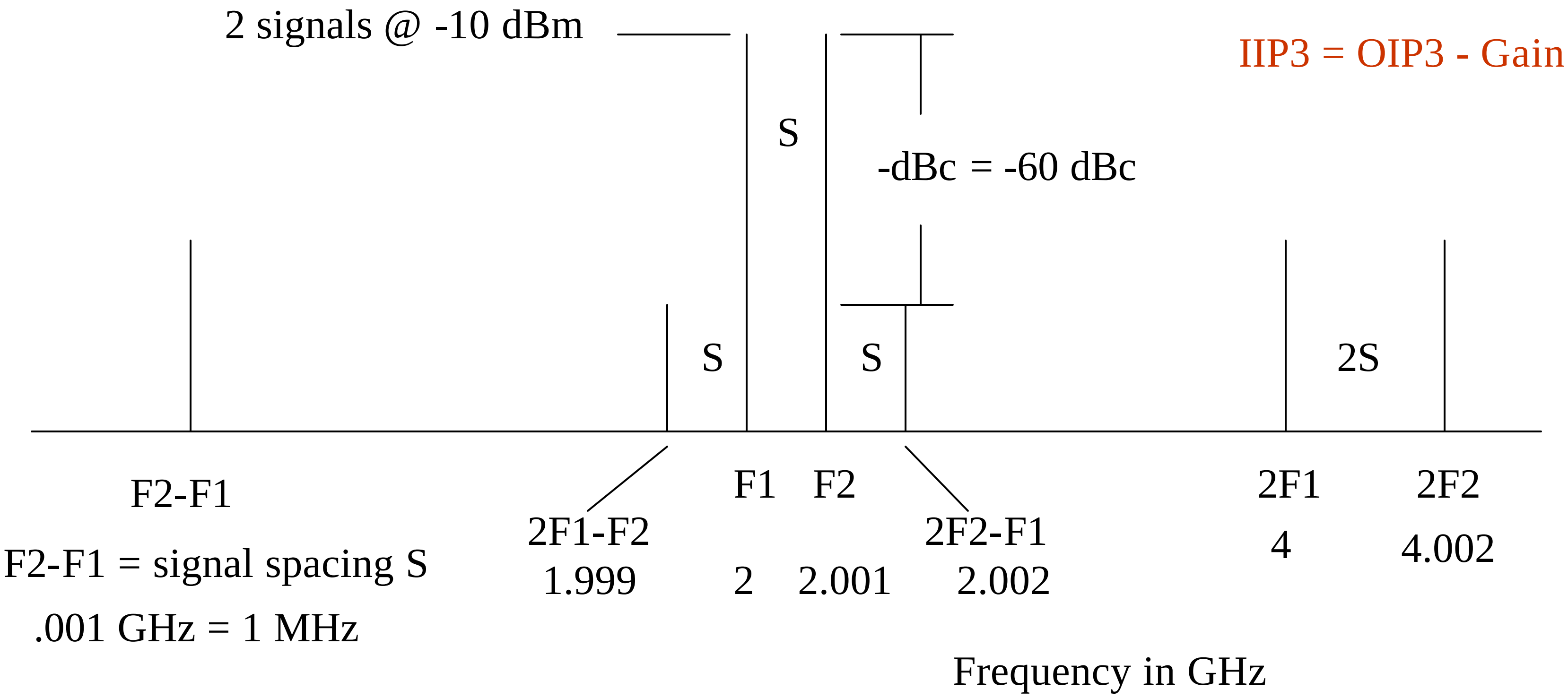
Measured
S21=19 dB
S11 = -9 dB
S22=-10dB
NF=0.28dB

How Are Third Order Products Produced?

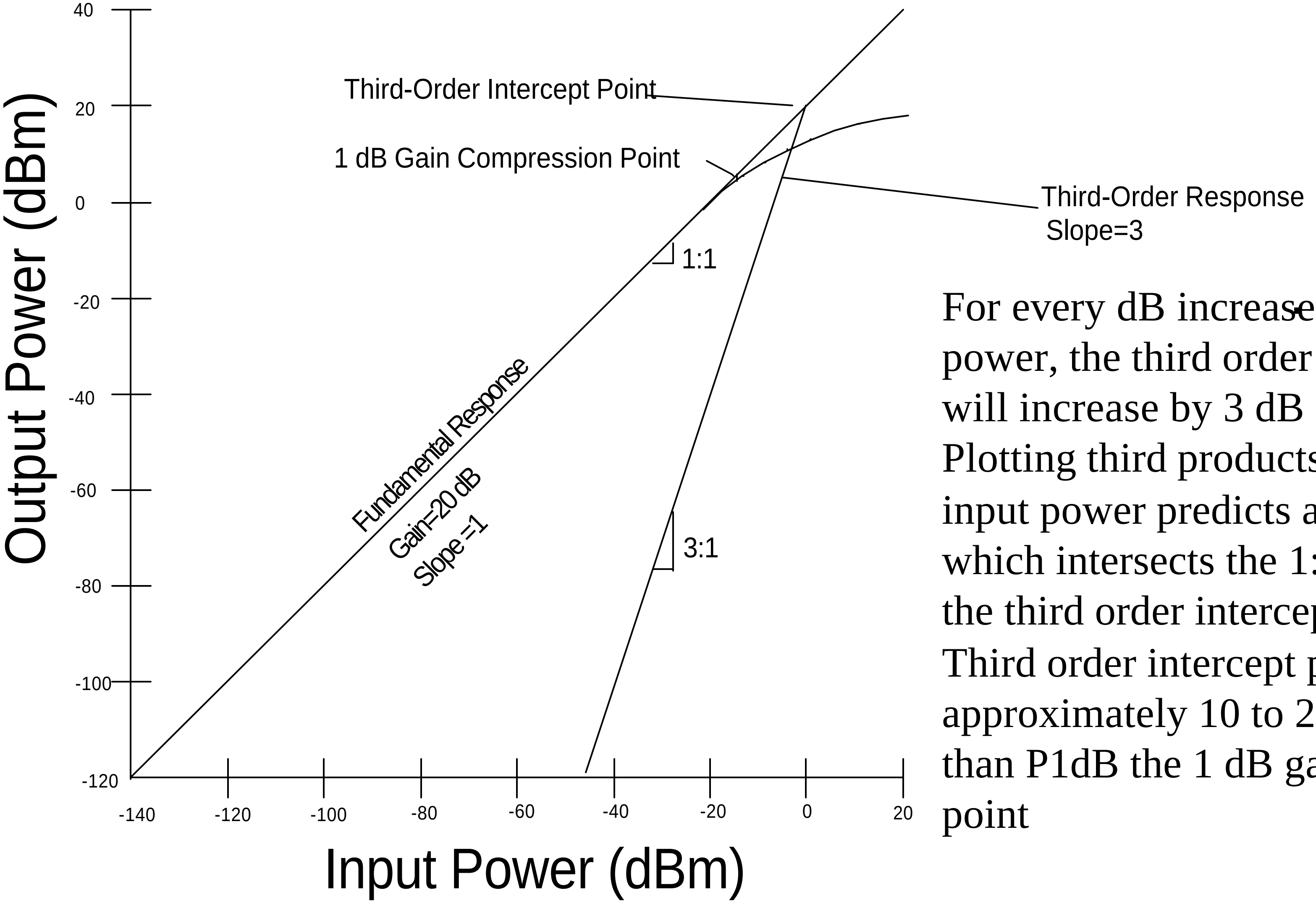
OIP3 = Pout + dBc/2

+20dBm = -10 dBm + 30dB

IIP3 = OIP3 - Gain



Plotting the Third Order Response

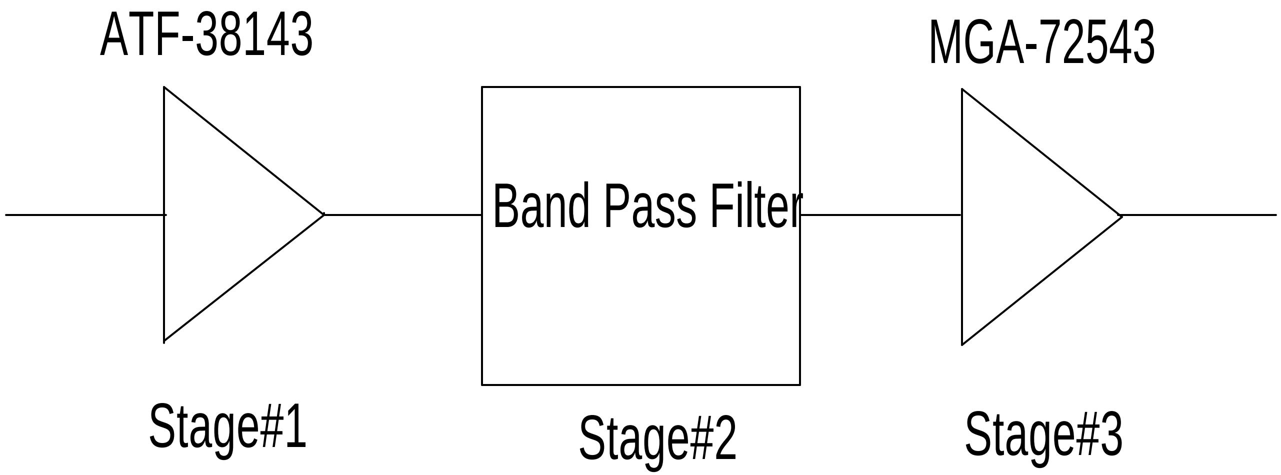


For every dB increase in input power, the third order products will increase by 3 dB

Plotting third products versus input power predicts a 3:1 response which intersects the 1:1 response at the third order intercept point

Third order intercept point will be approximately 10 to 20 dB higher than P1dB the 1 dB gain compression point

Cascade IP3 Calculation



	Stage#1	Stage#2	Stage#3
OIP3	+21dBm(125.9)	∞ dBm(∞)	+25 dBm(316.2)
Gain	15 dB (31.62)	-3 dB (.5)	15 dB (31.62)

$$\frac{1}{OIP3} = \frac{1}{OIP3_1 \bullet G_2 \bullet G_3} + \frac{1}{OIP3_2 \bullet G_3} + \frac{1}{OIP3_3}$$

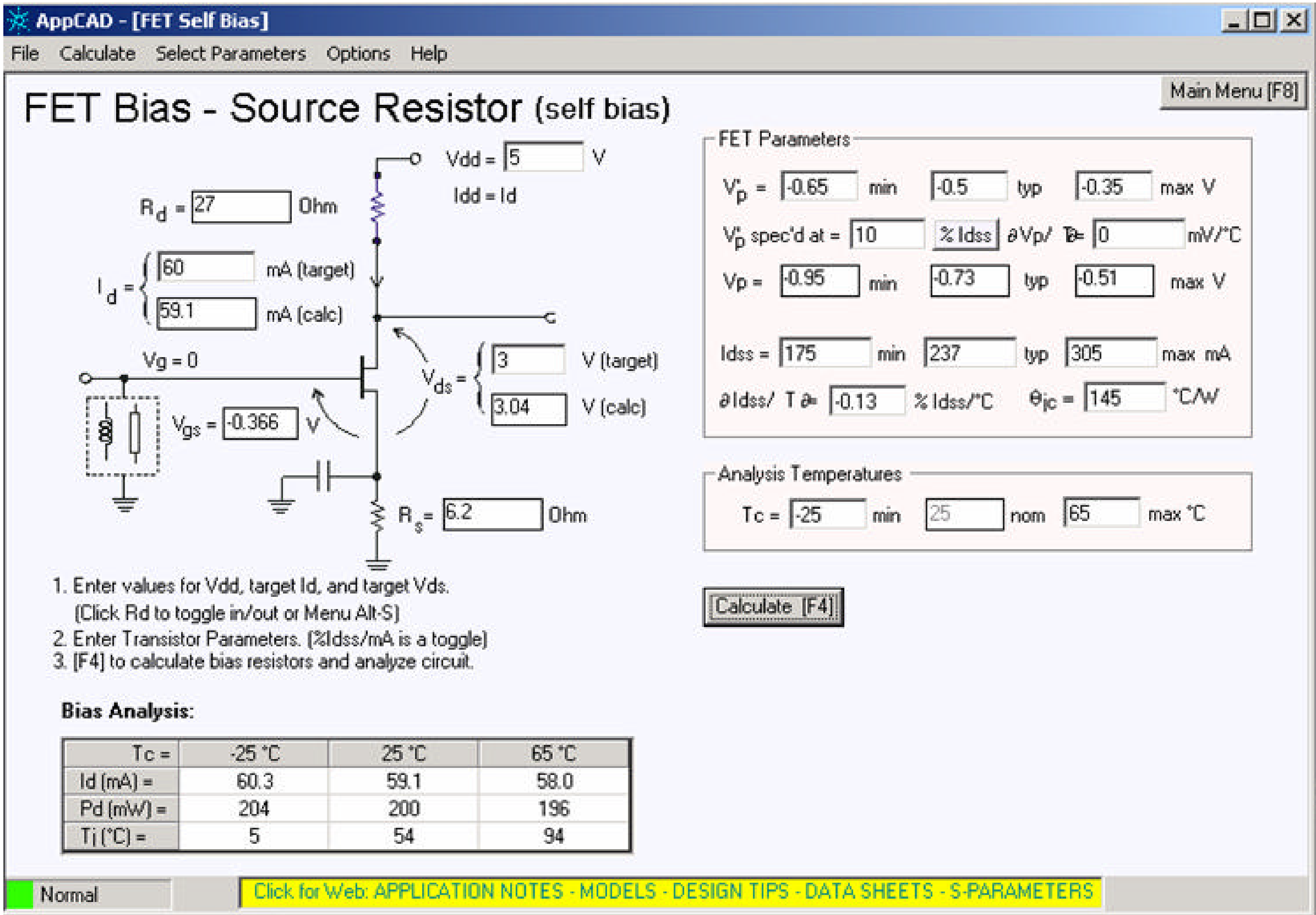
$$\frac{1}{OIP3} = \frac{1}{(125.9)(.5)(31.62)} + \frac{1}{(\infty)(31.62)} + \frac{1}{316.2}$$

$OIP3 = 273.075 = 24.4$ dBm , $IIP3 = 24.4 - 33 = -8.6$ dBm

Output Intercept Point Comparison

Frequency	Manufacturer	Device	OIP3
144 MHz	HB	3N211	+18 dBm
	Janel 144 PB	3N204	+19.5 dBm
	WD5AGO	ATF-33143	+22.5 dBm
432 MHz	ARR	3N204	+4 dBm
	HB	NE24483	+18 dBm
	WD5AGO	ATF-33143	+22.5 dBm

Using AppCAD to Calculate Bias Resistors



Summary

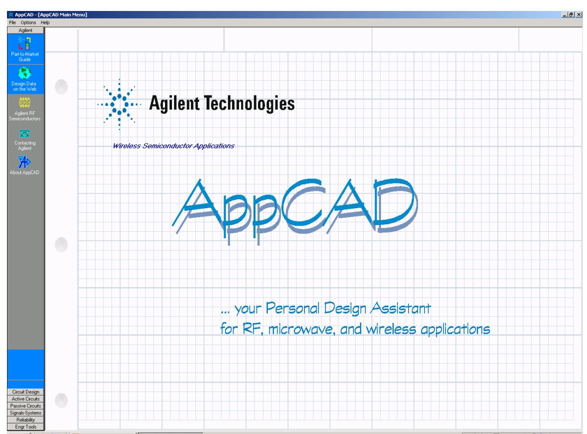
The older ceramic packaged FETs are being replaced by smaller surface mount plastic packaged devices.

Designing a stable low noise amplifier at VHF and UHF is certainly a challenge

Today’s LNA noise figures are limited more by circuit losses than device noise figures

Try AppCAD!

It’s Free!



Thank You!